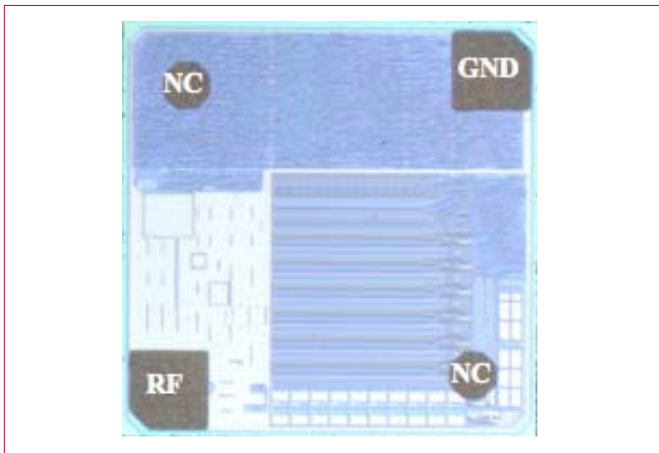# Higgs™-2
EPC Class 1 Gen 2 RFID Tag IC

HIggs-2 is a highly integrated single chip UHF RFID Tag IC. The chip conforms to the EPCglobal Class 1 Gen 2 specifications and provides state-of-the-art performance for a broad range of UHF RFID tagging applications.

Higgs-2 operates at extremely low power levels yet still provides sufficient backscatter signal to read tags at extended range. Higgs-2 can also be programmed at low RF power and, in conjunction with a custom command, be programmed at high speed. Higgs-2 is implemented in a low cost CMOS process and uses proven and cost effective EEPROM technology.

Higgs-2 features 4 unique memory maps that allow the IC to be tailored for different applications and use cases.

Features

❯ EPCglobal Gen2 certification for conformance and interoperability (V 1.0.9) as well as ISO/IEC 18000-6c

❯ Worldwide operation in the RFID UHF bands (860-960 MHz), allowing a tag to be used across the globe

❯ 192-Bits of Nonvolatile Memory, configurable in 4 different memory maps
  ❯ 96-bit EPC, 32-bit Access & 32-bit Kill Passwords
  ❯ 96-bit EPC, 32-bit Unique TID, 32-bit Kill Password
  ❯ 96-bit EPC, 64-bit User
  ❯ 128-bit EPC, 32-bit Kill Password

❯ Optional pre-programming with a unique, unalterable 32-bit serial number

❯ Supports all Mandatory and Optional Commands except for Block Erase/Write

❯ Custom Command for high speed programming; 30 tags typical per second for the 96-bit EPC number

❯ Low power operation for both read and program

❯ Long operating range, up to 10m with appropriate antenna

Applications

❯ Supply Chain Management

❯ Distribution Logistics

❯ Product Authentication

❯ Asset Inventory and Tracking

❯ Baggage Handling and Tracking

❯ Item Level Tagging

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Operating Conditions & Electrical Characteristics

Symbol	Parameter	Conditions / Capability	Min	Typ	Max	Units
Operating Conditions						
T_A	Operating Temperature		-50		+85	°C
f_{in}	Operating Frequency		860		960	MHz
Electrical Characteristics						
S_R	Sensitivity during Read	Reading	-11	-14		dBm
S_P	Sensitivity during programming	Programming	-6	-10		dBm
R_P	Equivalent input parallel resistance	At -14 dBm input power		1500		Ohms
C_P	Equivalent input parallel Capacitance	At -14 dBm input power		1.2		pF
D_{ret}	Data Retention	From date of manufacturer, at 25C		10		Years
P_{cycl}	Programming Cycles			10000		Cycles

Memory Maps

Alien H2 supports 4 different memory maps. The table below summarizes the different memory maps. The default map is the standard configuration unless the customer requests a different memory map. Customers have the ability to change from the Default map to either Map-1 or Map-2. This can be performed using the Custom command Load Image. Map-0 allows for Unique IDs and can only be set by Alien Technology® at the factory. Upon customer request Alien Technology can also program Unique IDs.

Bank	Address		Memory	Default	Map 0	Map 1	Map 2
User	00h - 3Fh	User	NVM	0	0	64	0
TID	50h - 6Fh	Unique Tag ID NVM	NVM	0	32	0	0
	20h - 4Fh	Device Configuration	NVM	48	48	48	48
	00h - 1Fh	TID EPC/TMD/TMDID/TMN	ROM	32	32	32	32
EPC	20h - 7Fh	EPC #	NVM	96	96	96	128
	10h - 1Fh	EPC-PC	NVM	16	16	16	16
	00h - 0Fh	EPC-CRC	RAM	16	16	16	16
Reserved	20h - 3Fh	RES-Access Pwd, EPC optional	NVM	32	0	0	0
	00h - 1Fh	RES-Kill Pwd	NVM	32	32	0	32

Table 1: Memory Map configurations

Ordering Information

Part	Model Number	Description
Higgs-2 IC	ALC-350-S	JEDEC MO-283 Variant AB Strap
	ALC-350-W-GS	Bumped, Tested, Ground & Sawn Wafer (8 inch) on UV Tape Mounted on Disco Metal Film Frame
	ALC-350-W-SOT	SMD Package: SOT-323

July 2008